AMENDMENTS TO THE CLAIMS:

1. - 19. (Canceled)

20. (Currently Amended) A circuit, comprising:

circuit elements;

scan chain elements to contain a vector for selective application to said circuit elements;

a vector memory for containing a configuration vector which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;

a multiplexer to select said configuration vector for loading into said scan chain elements, wherein said multiplexer is controlled by a finite state machine, and wherein the finite state machine includes sleep, standby and at least one other value;

a clock generator to clock said configuration vector into said scan chain elements;

a circuit for receiving a test vector for clocking into said scan chain elements;

wherein said multiplexer is configured to select between said configuration vector and said test vector for loading into said scan chain elements; and

wherein said clock generator is configured to clock said selected vector into said scan elements.

21. (Previously Presented) The circuit of claim 20 further comprising a sleep mode detector to configure said multiplexer to select said configuration vector and to operate said clock generator to clock said configuration vector into said scan chain elements when a sleep mode of said circuit is detected.

22. (Previously Presented) The circuit of claim 21 further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements.

23. (Currently Amended) A circuit, comprising:

circuit elements;

scan chain elements to contain a vector for selective application to said circuit elements;

a test input for receiving a test vector;

a vector memory for containing a configuration vector which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;

a first multiplexer to select between said configuration vector and said test vector for loading into said scan chain elements wherein said first multiplexer is controlled by a finite state machine, and wherein the finite state machine comprises sleep, standby and at least one other mode;

a second multiplexer to select between a test enable signal and a configuration vector enable signal and output a selected enable signal, said selected enable signal operable for enabling said scan

chain elements to select between [[said]] a first selected vector and a normal operation mode data vector for loading into said scan chain elements; and

a clock generator generating a clocking signal to clock [[said]] a second selected vector into said scan chain elements.

24. (Previously Presented) The circuit of claim 23 further comprising a sleep mode detector to configure said multiplexer to select said configuration vector and to operate said clock generator to clock said configuration vector into said scan chain elements when a sleep mode of said circuit is detected.

25. (Previously Presented) The circuit of claim 24 further comprising a scan chain turn off circuit to turn off a clock to said scan chain elements after said configuration vector has been applied to said circuit elements.

26. (Previously Presented) The circuit of claim 23 further comprising:

a scan chain turn off circuit operable for disabling a clock signal to said scan chain elements after said configuration vector has been loaded into said scan chain elements.

27. (Previously Presented) The circuit of claim 23 wherein during a sleep mode, said configuration vector enable signal is only activated for a predetermined number of cycles of said clock generator equal to or less than the number of said scan chain elements.

28. (Currently Amended) The circuit of claim 26 further comprising:

[[a]] the finite state machine operable for receiving a sleep mode signal defining said sleep mode, and in response thereto, generating said configuration vector signal, controlling said first and second multiplexers, and in response to said sleep mode signal, and disabling said clocking signal to said scan chain elements after said configuration vector has been loaded into said scan chain elements.

29. (Previously Presented) The circuit of claim 28 wherein said finite state machine is further operable for generating said configuration vector enable signal and activating said configuration vector control signal for a period of time less than said sleep mode.

30. (Previously Presented) The circuit of claim 28 wherein said finite state machine is further operable for generating a clock gating signal that disables said clocking signal to said scan chain elements.

31. (Previously Presented) The circuit of claim 23 wherein said configuration vector comprises at least two data and each data in said configuration vector is sequentially loaded into said scan chain elements in response to said clocking signal.

32. (Currently Amended) A circuit, comprising:

circuit elements;

scan chain elements to contain a vector for selective application to said circuit elements;

means for receiving a test vector;

means for storing a configuration vector which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;

means for selecting between said configuration vector and a test vector for loading into said scan chain elements;

means for a [[second]] multiplexer to select between a test enable signal and a configuration vector enable signal and output a selected enable signal, said selected enable signal operable for enabling said scan chain elements to select between a [[said]] first selected vector or a normal operation mode data vector for loading into said circuit elements wherein said multiplexer is controlled by a finite state machine, and wherein the finite state machine comprises sleep, standby and at least one other mode; and

means for generating a clocking signal to clock a [[said]] second selected vector into said scan chain elements.

33. (Canceled)

34. (Currently Amended) A method for reducing leakage currents in a circuit, the method comprising:

providing circuit elements;

providing scan chain elements to contain a vector for selective application to said circuit elements;

receiving a configuration vector from memory which, when applied to said circuit elements, configures said circuit elements into a state in which a leakage current is reduced;

selecting between said configuration vector and a test vector for loading into said scan chain elements and outputting a first selected vector wherein the selection is controlled by a finite state machine, and wherein the finite state machine comprises sleep, standby and other modes;

selecting between a test enable signal and a configuration vector enable signal and outputting a selected enable signal;

receiving said selected enable signal and said first selected vector, and in response thereto, selecting between said first selected vector and a normal operation mode data vector for loading into said scan chain elements; and

generating a clocking signal to clock said vector selected by said selected enable signal into said scan chain elements and applying said clocked vector to said circuit elements.

35. (Previously Presented) The method of claim 34 further comprising:

configuring said multiplexer to select said configuration vector and to operate said clock generator to clock said configuration vector into said scan chain elements when a sleep mode of said circuit is detected.

36. (Previously Presented) The method of claim 35 further comprising:

activating during the sleep mode said configuration vector enable signal only for a predetermined number of cycles of said clock generator equal to or less than the number of said scan chain elements.